REMARKS

Applicant respectfully requests reconsideration of the subject application as amended. In response to the Office Action mailed 5/19/06, Applicant is submitting the following argument in response to the Examiner's rejections to the newly submitted claims 21-28.

In the Office Action mailed 5/19/06, the Examiner has rejected claims 21, 23, 25 and 27 under 35 U.S.C. §102(b) as being anticipated by Avnon et al. (U.S. Patent 5,559,977; "Avnon") and the remaining claims 22, 24, 26 and 28 under 35 U.S.C. §103(a) as being unpatentable over Avnon in view of Halfhill ("SiByte Reveals 64-Bit Core for NPUs"). Applicant has considered the reasons noted by the Examiner for the rejections and responds as follows.

Avnon discloses that in some special cases the floating-point pipeline is capable of executing a floating-point pair of instructions. Further, that the floating-point unit **110** employs a technique referred to as "safe instruction recognition" to determine whether operands supplied to an instruction have the potential of generating a floating-point exception. If an exception is possible on a single floating-point instruction, the floating-point pipeline of Fig. 4 stalls subsequent floating-point instructions in the E stage. If an exception is possible on a pair of floating-point instructions that were issued together, subsequent integer instructions are stalled in the D2 stage, while subsequent floating-point instructions are stalled in the E stage. (Avnon at col.7, line 63 – col. 8, line10).

Avnon further discloses that if there is a single or pair of floating-point instructions that are determined to be unsafe in the floating-point pipeline, FIRC **201** stalls the subsequent floating-point microinstruction at the E stage in the pipeline (Avnon at col. 9, lines 16-19). Also, if a floating-point instruction pair is issued, FIRC **201** stalls the integer execution pipeline at the D2 stage to prevent integer instructions from reaching the E stage (Avnon at col. 9, lines 24-26). It should be noted that if a single floating-point instruction is labeled unsafe, the integer pipeline need not stall (Avnon at col. 9, lines 33-35).

Thus, Applicant submits that Avnon teaches the stalling of floating-point pipeline when one or pair of floating-point instructions are determined to be unsafe. However, for the integer pipeline, the integer pipeline is stalled with the pair of floating-point instructions, but not stalled with a single floating-point instruction.

Applicant's independent claims 21 and 25 recite inhibiting of a co-issuance of an integer instruction to the integer pipeline when the integer instruction is subsequent to a first floating-point instruction. Thus, an integer instruction subsequent to the first floating-point instruction is inhibited from co-issuance, whereas in Avnon, the integer pipeline is not stalled with a single floating-point instruction.

Additionally, Applicant's independent claims 21 and 25 recite inhibiting co-issuance of a second floating-point instruction that follows the first floating-point instruction in program order, if the first floating-point instruction is not a short latency floating-point instruction, to ensure that the second floating-point instruction does not graduate prior to the exception determination for the first floating point instruction. However, the claims recite not to inhibit the second floating-point instruction from co-issuance if the first floating-point instruction is a short latency floating-point instruction, since the second floating-point instruction will not graduate prior to the exception determination for the first floating-point instruction.

Applicant submits that Avnon teaches the stalling of the floating-point pipeline whether a single floating-point instruction or a floating-point instruction pair are issued, which is contrary to the Applicant's claimed condition of not inhibiting the second floating-point instruction from co-issuance if the first floating-point instruction is a short latency floating-point instruction. The Examiner has stated that a "safe floating-point instruction is a short latency floating-point instruction since it has been determined to be not an exception causing floating point instruction." However, Applicant has not found such a statement disclosed in Avnon and, accordingly, requests the Examiner to point to the specific language in Avnon to support the Examiner's statement. Thus, Applicant submits that the independent claims 21 and 25 are not anticipated by Avnon.

Accordingly, for the reasons noted above, Applicant submits that claims 21, 23, 25 and 27 distinguish over Avnon. Similarly, Applicant applies the same argument to

distinguish claims 22, 24, 26 and 28 over Avnon and Halfhill, as well, in responding to the 35 U.S.C. §103(a) rejection.

Accordingly, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. §102(b) and 35 U.S.C. §103(a) rejections and allow pending claims 21-28.

Furthermore, in order to respond to the outstanding office action, Applicant is also submitting a petition for two-months extension of time under a separate cover.

Additionally, a new power of attorney is being submitted herewith, in order to associate this application with Customer Number 51472.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

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